T Flip Flop:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity T\_FF is

Port ( T : in STD\_LOGIC;

CLK : in STD\_LOGIC;

RST : in STD\_LOGIC;

Q : out STD\_LOGIC);

end T\_FF;

architecture Behavioral of T\_FF is

signal tmp : std\_logic := '0';

begin

process(RST,T,CLK)

begin

if(rst='1')then

tmp<='0';

elsif(rising\_edge(clk))then

if(T='1')then

tmp<= not tmp;

end if;

end if;

end process;

q<=tmp;

end Behavioral;

Decade Counter:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_unsigned.ALL;

entity decade\_ctr is

Port ( CLK : in STD\_LOGIC;

RST : in STD\_LOGIC;

Q : out STD\_LOGIC\_VECTOR (3 downto 0));

end decade\_ctr;

architecture Behavioral of decade\_ctr is

component T\_FF is

Port ( T : in STD\_LOGIC;

CLK : in STD\_LOGIC;

RST : in STD\_LOGIC;

Q : out STD\_LOGIC);

end component;

signal b3,b2,b1,b0,flag : std\_logic := '0';

begin

tff\_0 : T\_FF port map(not flag,clk,flag,b0);

tff\_1 : T\_FF port map(not flag,not b0,flag,b1);

tff\_2 : T\_FF port map(not flag,not b1,flag,b2);

tff\_3 : T\_FF port map(not flag,not b2,flag,b3);

flag <= (b3 and not b2 and b1 and b0) or RST;

Q <= b3 & b2 & b1 & b0;

end Behavioral;